PTO/SB/08A (10-01)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	Not assigned yet 10/767,069
Filing Date	On even date herewith
First Named Inventor	S. SHUKURI
Art Unit	Not assigned yet
Examiner Name	Not assigned yet
Attorney Docket Number	501.42645VX1

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
DR		5,768,192	6/16/98	Eitan	
		5,966,603	10/12/99	Eitan	
		6,011,725	1/4/00	Eitan	
		6,180,538	1/30/01	Hallival et al.	
		5,408,115	4/18/95	Chang	
DR		5,969,383	10/19/99	Chang et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]–Number[4]–Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

OTHER PRIOR ART—NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
DR		"Can NROM, a 2 Bit, Trapping Storage NVM Cell, Give a Real Challenge to Floating Gate Cells?" Eitan et al., Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, Tokyo, 1999, pp.522-524	
		"High Speed Program/Erase Sub 100 nm MONOS Memory Cell" Fujiwara et al., pp.75-77	
		"A Novel Flash Memory Device with Split Gate Source Side Injection and ONO Charge Storage Stack (SPIN)" Chen et al., 1997 Symposium on VLSI Technology Digest of Technical Papers, pp. 63-64	
DR		"Twin MONOS Cell with Dual Control Gates" Hayashi et al., Symposium on VLSI Technology Digest of Technical Papers, pp. 122-123	

Examiner Signature		Date Considered	12/13/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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DV		6,335,554		01-01-2002	Yoshikawa	
DV		6,632,714		10-14-2003	Yoshikawa	

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OTHER PRIOR ART—NON PATENT LITERATURE DOCUMENTS

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DV		Takaaki NOZAKI, et al., A 1 Mbit EEPROM with MONOS Memory Cell for Semiconductor Disk Application, 1990 Symposium on VLSI Circuits, 1990 IEEE, (pp 101-102)	

Examiner Signature		Date Considered	12/13/04

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